

METHOD OF ENLARGING CONTACT AREA OF A GATE ELECTRODE, SEMICONDUCTOR
DEVICE HAVING A SURFACE-ENLARGED GATE ELECTRODE, AND METHOD OF
MANUFACTURING THE SAME

Application No. NEW - Attorney Docket No. SEC.1134

Inventor(s): Chan-Hyung CHO et al.

FIG. 1A

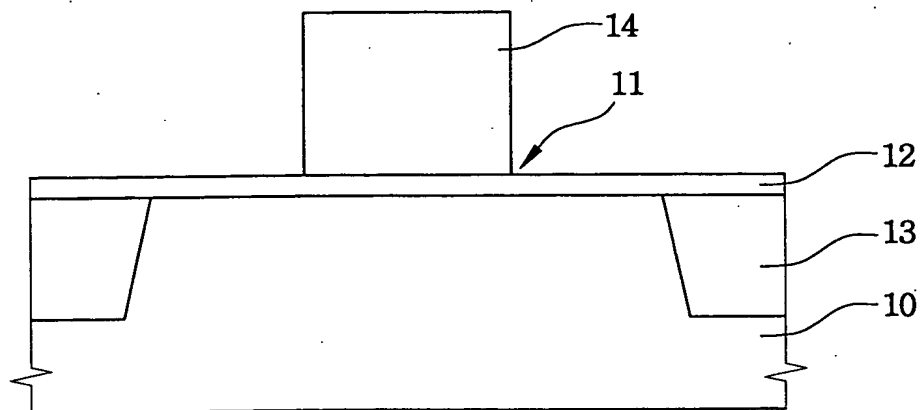
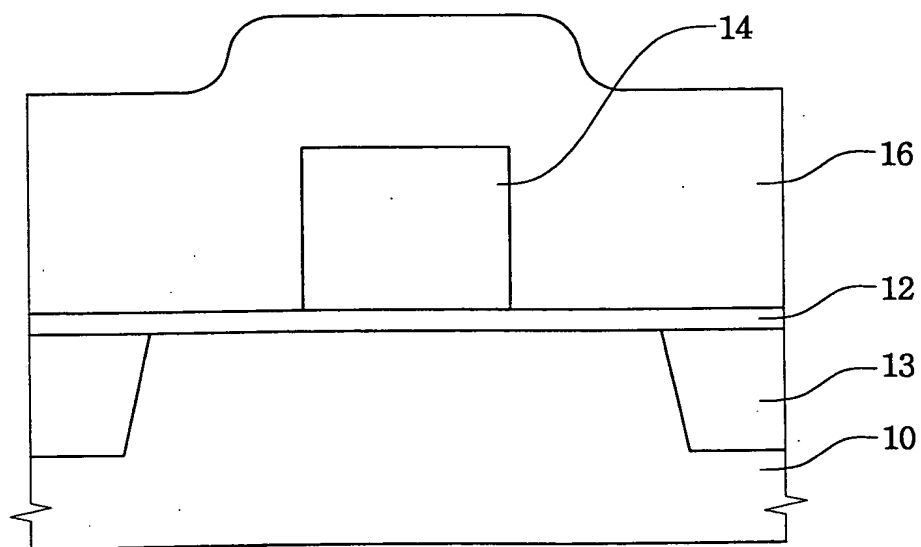


FIG. 1B



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FIG. 1C

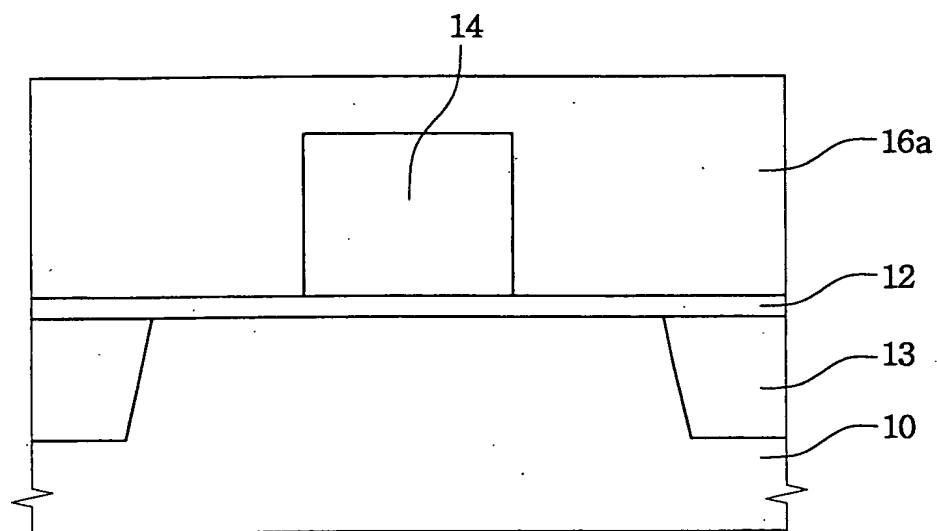
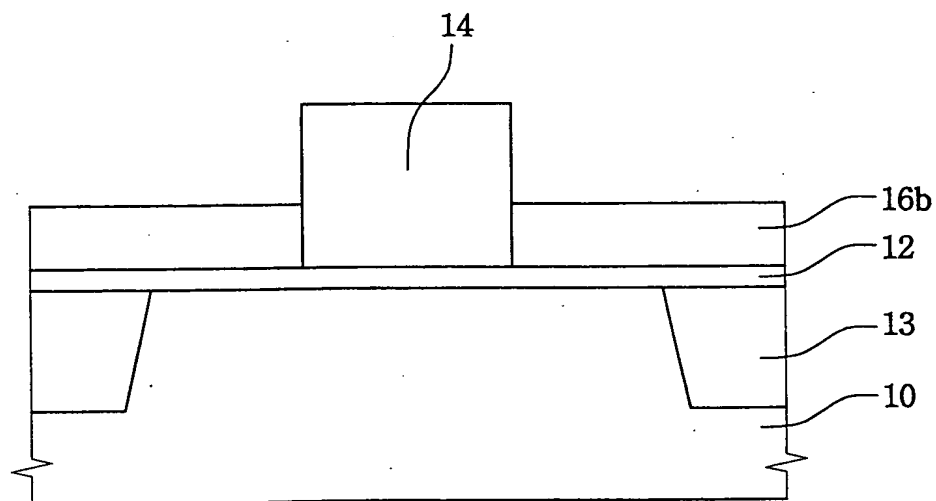


FIG. 1D



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FIG. 1E

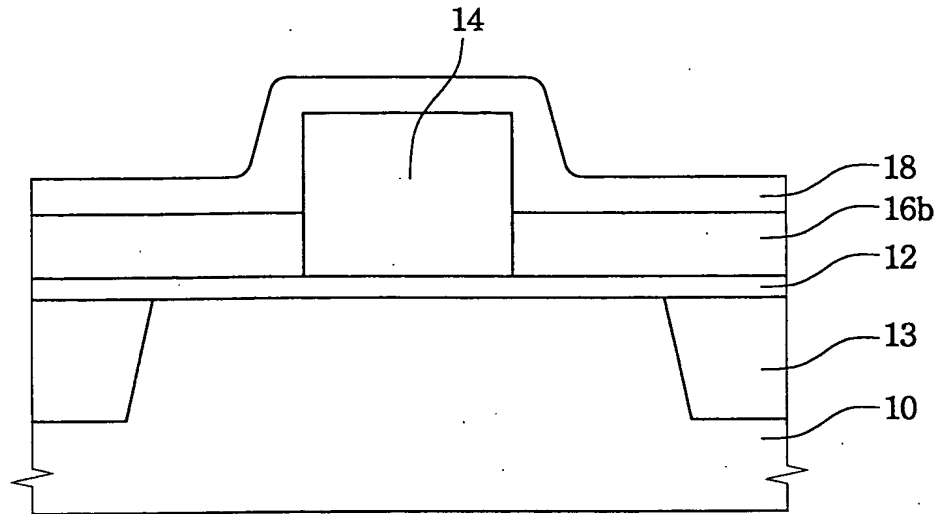
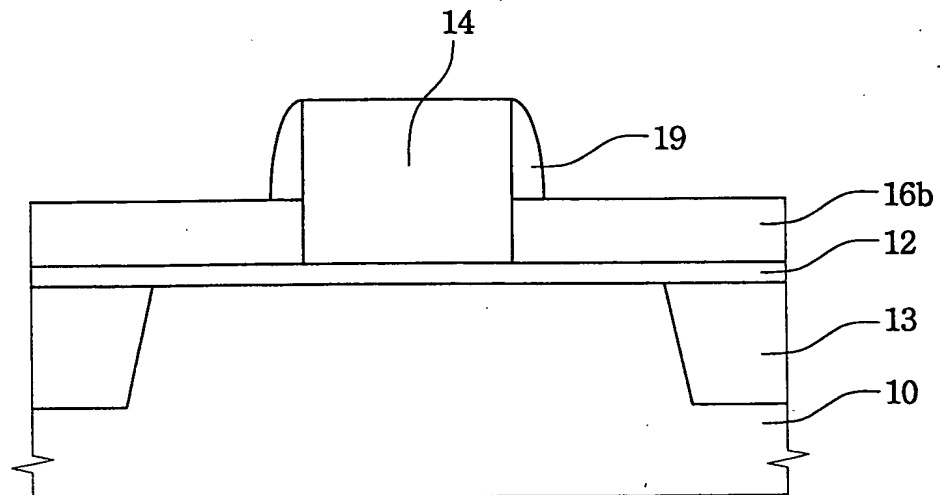


FIG. 1F



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FIG. 1G

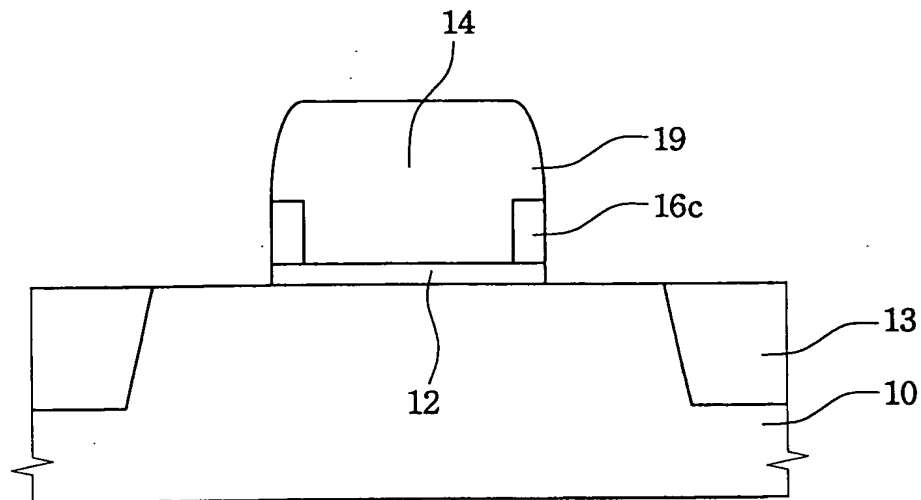
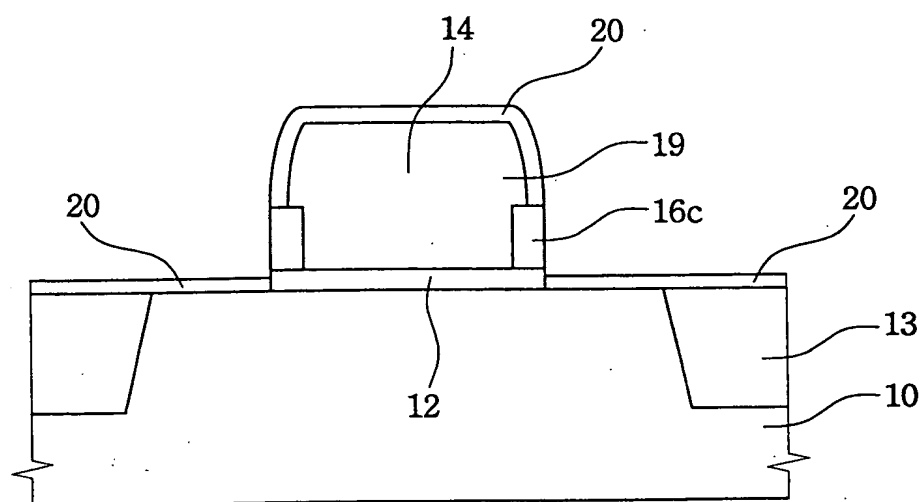


FIG. 1H



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This cross-sectional view shows a central dome-shaped structure (14) with a top surface (19) and side surface (20). The dome is supported by a base layer (12) which has two side regions (22a, 22b). The base layer is situated on a substrate (10) with a top surface (13). Arrows indicate light incident from the top and bottom, and a label 16c points to the side of the dome.

This cross-sectional view shows a semiconductor device with a central cavity 14. A top layer 20 is formed over the cavity. A layer 16c is located on the side walls of the cavity. The device is mounted on a substrate 10, which has a layer 13 and a layer 12. The device is connected to the substrate by contacts 22a and 22b. A layer 23 is formed on the top surface of the device.

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This cross-sectional view shows a semiconductor device with a central gate structure. The device is built on a substrate 10, which has a base layer 12 and a top layer 13. A central gate stack 14 is formed on the top layer 13, consisting of a gate dielectric 19 and a gate electrode 20. The gate stack 14 is flanked by two side regions 24, which are part of a larger structure 16c. The side regions 24 are separated from the central gate stack 14 by gaps 22a and 22b. The side regions 24 are also separated from the substrate 10 by a layer 26. The top layer 13 is shown with a break on the right side, indicated by a jagged line. Arrows at the top indicate a downward force or pressure applied to the top layer 13.

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FIG. 1M

